IN THE CLAIMS

Please amend claims 24 and 27-29 and add new claim 34 as set forth below.

1. - 23. (Canceled)

24. (Currently Amended) A semiconductor device comprising:

a plurality of first memory cells for storing either one of first information or second information, arranged at points of intersection between a plurality of word lines and a first data line;

a plurality of first dummy cells for storing the first information, arranged at points of intersection between said plurality of word lines and a first dummy data line;

a plurality of second dummy cells for storing the second information, arranged at points of intersection between said plurality of word lines and a second dummy data line;

a plurality of first redundancy cells arranged at points of intersection between said plurality of word lines and a first redundancy data line;

a plurality of second redundancy cells arranged at points of intersection between said plurality of word lines and a second redundancy data line; and

a plurality of third redundancy cells arranged at points of intersection between said plurality of word lines and a third redundancy data line,

wherein when one of said plurality of first memory cells has a defect, said first redundancy data line replaces said first data line,

wherein when one of said plurality of first dummy ~~memory~~ cells has a defect, said second redundancy data line replaces said first dummy data line, and

wherein when one of said plurality of second dummy ~~memory~~ cells has a defect, said third redundancy data line replaces said second dummy data line.

25. (Previously Presented) A semiconductor device according to claim 24,

wherein said first and second redundancy data lines are arranged between said first data line and said first dummy data line.

26. (Previously Presented) A semiconductor device according to claim 25, further comprising:

a first multiplexer coupled to said first data line;

a first dummy multiplexer coupled to said first and second dummy data lines;

a first redundancy multiplexer coupled to said first redundancy data line; and

a second redundancy multiplexer coupled to said second and third redundancy data lines.

27. (Currently Amended) A semiconductor device according to claim 26,

wherein when said second ~~first~~ redundancy data line replaces said first dummy data line and said second dummy data line which has no memory cell defect is not replaced ~~due to a memory cell defect~~, said first dummy multiplexer selects said second dummy data line and said second redundancy multiplexer selects said second redundancy data line, and

when said second redundancy data line replaces said first dummy data line and said third redundancy data line replaces said second dummy data line, said second redundancy ~~first dummy~~ multiplexer selects said second and third

redundancy ~~dummy~~ data lines and said first dummy multiplexer does not select said first and second dummy data lines.

28. (Currently Amended) A semiconductor device comprising:

a plurality of first memory cells for storing either one of first information or second information, arranged at points of intersection between a plurality of word lines and a first data line;

a plurality of first dummy cells for storing the first information, arranged at points of intersection between said plurality of word lines and a first dummy data line;

a plurality of second dummy cells for storing the second information, arranged at points of intersection between said plurality of word lines and a second dummy data line;

a plurality of first redundancy cells arranged at points of intersection between said plurality of word lines and a first redundancy data line; and

a plurality of second redundancy cells arranged at points of intersection between said plurality of word lines and a second redundancy data line,

wherein when one of said plurality of first memory cells, first dummy cells, or second dummy cells has a defect,

said first redundancy data line replaces one of said first data line, first dummy data line, or second dummy data line connected to the memory ~~cells~~ cell having the defect.

29. (Currently Amended) A semiconductor device according to claim 28, further comprising:

a plurality of second memory cells for storing either one of the first information or the second information, arranged at points of intersection between a plurality of word lines and a second data line;

a plurality of third dummy cells for storing the first information, arranged at points of intersection between said plurality of word lines and a third dummy data line;

a plurality of fourth dummy cells for storing the second information, arranged at points of intersection between said plurality of word lines and a fourth dummy data line;

a plurality of third redundancy cells arranged at points of intersection between said plurality of word lines and a third redundancy data line; and

a plurality of fourth redundancy cells arranged at points of intersection between said plurality of word lines and a fourth redundancy data line,

wherein when one of said plurality of second memory cells, third dummy cells, or fourth dummy cells has a defect, said third redundancy data line replaces one of said second data line, third dummy data line, or fourth dummy data line connected to the memory ~~cells~~ cell having the defect.

30. (Previously Presented) A semiconductor device according to claim 29, further comprising:

a first multiplexer coupled to said first data line;

a second multiplexer coupled to said second data line;

a first dummy multiplexer coupled to said first and second dummy data lines;

a second dummy multiplexer coupled to said third and fourth dummy data lines;

a first redundancy multiplexer coupled to said first and second redundancy data lines; and

a second redundancy multiplexer coupled to said third and fourth redundancy data lines.

31. (Previously Presented) A semiconductor device according to claim 28,

wherein said first and second redundancy data lines are arranged between said first data line and said first dummy data line.

32. (Previously Presented) A semiconductor device according to claim 24,

wherein each of said pluralities of first memory cells, first dummy cells, second dummy cells, first redundancy memory cells, second redundancy memory cells, and third redundancy memory cells has a magnetic tunnel junction device.

33. (Previously Presented) A semiconductor device according to claim 28,

wherein each of said pluralities of first memory cells, first dummy cells, second dummy cells, first redundancy memory cells, and second redundancy memory cells has a magnetic tunnel junction device.

34. (New) A semiconductor device according to claim 30,

wherein when the first redundancy data line replaces the first dummy data line and the second redundancy data line replaces the second dummy data line, the dummy multiplexer

does not select the first and second dummy data lines and the first redundancy multiplexer selects the first and second redundancy data lines, and

wherein when the first redundancy data line replaces the first data line and the second redundancy data line replaces the second dummy data line, the first multiplexer does not select the first data line, the first dummy multiplexer selects the first dummy data line, and the first redundancy multiplexer selects the first and second redundancy data lines.